UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/677,191 | 10/02/2003 | Gregory S. Glenn | PD-02-0360/11836 (21797-0 | 8302 |

7590 03/30/2007

Carmen Santa Maria
McNees Wallace & Nurick LLC
100 Pine Street
P.O. Box 1166
Harrisburg, PA 17108-1166

| EXAMINER | |
|---|---|
| TRINH, THANH TRUC | |
| **ART UNIT** | **PAPER NUMBER** |
| 1753 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/30/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/677,191 | GLENN, GREGORY S. | |
| | Examiner | Art Unit | |
| | Thanh-Truc Trinh | 1753 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/02/2003, 1/11/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 recites the limitation "the substrate" in lines 3-4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 13 renders indefinite by the phrase "... of claim 11... as set forth in claim 10", it is unclear whether the claim is depend on claim 11 or claim 10.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8, 10-13, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Muller (US Patent 6452086).

See Figures 1-3.

Regarding claim 1, Müller discloses a solar cell structure having a solar cell unit structure 8 comprising a heat sink (5b and 5c); a solar cell (or solar cell arrangement 4) having a front side, a back side, and a solar-cell projected area coverage on the heat sink, wherein the solar cell comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated; and an intermediate structure (or substrate 1) disposed between and joined to the back side of the solar cell and to the heat sink, and having an intermediate-structure projected area coverage on the heat sink, wherein the intermediate structure comprises a by-pass diode 12 (including anode 2 and cathode 3) having a diode projected area coverage on the heat sink. (See Figures 1-2). Further, contacts 5b and 5c are made of metal, therefore they can function as a heat sink. Since Muller teaches the limitations of the instant claim, the reference is deemed to be anticipatory.

Regarding claim 2, Müller discloses the diode projected area coverage on the heat sink is less than the solar cell projected area coverage on the heat sink, and wherein the intermediate structure further comprises a substrate coplanar with the by-pass diode. (See Figure 1).

Regarding claim 3, Müller discloses the diode projected area coverage on the heat sink is less than the solar-cell projected area coverage on the heat sink, and wherein the intermediate structure further comprises a substrate coplanar with the by-

pass diode and having a substrate projected area coverage on the heat sink such that the diode projected area coverage on the heat sink and the substrate projected area coverage on the heat sink taken together are not less than the solar cell projected area coverage on the heat sink. (See Figure 1)

Regarding claim 4, Müller discloses the diode projected area coverage on the heat sink is less than the solar cell projected area coverage on the heat sink, wherein the substrate has a substrate notch, and wherein the by-pass diode is received into the substrate notch. (See Figure 1). It is the position of the examiner to consider the "notch" is a region in the substrate to have the diode. Muller teaches the substrate having a region for the by-pass diode as shown in Figure 1. Therefore Muller teaches the limitations of the instant claim, and the reference is deemed to be anticipatory.

Regarding claim 5, Müller discloses the intermediate-structure projected area coverage on the heat sink is not less than the solar cell projected area coverage on the heat sink. (See Figure 1)

Regarding claim 6, Müller discloses an intra-unit electrical connection structure operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. (See Figures 1-3). Muller teaches the intra-unit electrical connection structure comprising the electrical conductor 7 connecting the solar cell and

the diode at one end, and the n-doped substrate connecting the solar cell and the diode at the other end.

Regarding claim 7, Müller teaches the back side of the solar cell is substantially planar. (See Figure 1).

Regarding claim 8, Müller describes that the solar cell structure includes at least one additional solar cell unit structure (9) as set forth in claim 1, and further including a circuit electrical connection structure 7 operable to electrically interconnect each of the solar cell unit structures in series. (See Figures 1 and 3).

Regarding claim 10, Müller describes that the solar cell structure includes a joint 7 between the intermediate structure and the heat sink. (See Figure 3). The joint 7 in the reference is used to connect the heat sink (or the metal contact) of one solar cell unit to the other. Since the metal contact is directly connected to the diode, or the intermediate structure, therefore the joint 7 is inherently connecting the intermediate structure and the heat sink. The joint 7 is also a metallic trace and functioning as part of the electrical interconnection like the PC board disclosed by the Applicant. It is the Examiner's position to consider joint 7 being a PC board having metallic trace on the face thereof.

Regarding claim 11, Müller discloses a solar cell structure having a solar cell unit structure 8 comprising a heat sink (contact 5b and 5c); a solar cell 4 having a front side, a back side, and a solar-cell projected area coverage on the heat sink, wherein the solar cell inherently comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated; an intermediate structure 1 disposed between and joined to the back side of the solar cell and to the heat sink and having an intermediate-structure projected area coverage on the heat sink, wherein the intermediate structure comprises a by-pass diode having a diode projected area coverage on the heat sink that is less than the intermediate-structure projected area coverage on the heat sink, and a substrate coplanar with the by-pass diode and having a substrate projected area coverage on the heat sink such that the diode projected area coverage on the heat sink and the substrate projected area coverage on the heat sink taken together are not less than the solar-cell projected area coverage on the heat sink; and an intra-unit electrical connection structure operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. (See Figures 1-3)

Regarding claim 12, Müller describes the back side of the solar cell is substantially planar. (See Figure 1)

Regarding claim 13, Müller discloses a solar cell structure further including a circuit electrical connection structure (electrical conductor 7 and the doped substrate)

operable to electrically interconnect each of the solar cell unit structures in series. (See Figures 1, 3)

Regarding claim 15, Müller describes that the solar cell structure includes a joint 7 between the intermediate structure and the heat sink. (See Figure 3). The joint 7 in the reference is used to connect the heat sink (or the metal contact) of one solar cell unit to the other. Since the metal contact is directly connected to the diode, or the intermediate structure, therefore the joint 7 is inherently connecting the intermediate structure and the heat sink. The joint 7 is also a metallic trace and functioning as part of the electrical interconnection like the PC board disclosed by the Applicant. It is the Examiner's position to consider joint 7 being a PC board having metallic trace on the face thereof.

3. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Glenn (US Patent 6313396).

See Figure 1.

Regarding claim 1, Glenn discloses a solar cell structure having a solar cell unit structure comprising a heat sink 20; a solar cell (11 or 12 or 13) having a front side 29, a back side 21, a solar cell projected area coverage on the heat sink, wherein the solar cell comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated; and an intermediate structure (including all the layers between solar cells 11, 12, 13 and the heat sink) of

disposed between and joined to the back side of the solar cell and to the heat sink, and having an intermediate structure projected area coverage on the heat sink. The intermediate structure further comprises a by-pass diode 15 having a diode projected area coverage on the heat sink. (See Figure 1 and col. 4 lines 10-31, 62-67 and col. 5 lines 1-19)

Regarding claim 2, Glenn discloses the diode projected area coverage on the heat sink is less than the solar cell projected area coverage on the heat sink, and wherein the intermediate structure further comprises a substrate (bonding element 18, dielectric layer 16, conducting element 17...) coplanar with the by-pass diode 15. (See Figure 1).

Regarding claim 3, Glenn discloses the diode projected area coverage on the heat sink is less than the solar-cell projected area coverage on the heat sink, and the intermediate structure further comprises a substrate (bonding element 18 and dielectric layer 16, conducting element 17...) coplanar with the by-pass diode 15 and having a substrate projected area coverage on the heat sink such that the diode projected area coverage on the heat sink and the substrate projected area coverage on the heat sink taken together are not less than the solar cell projected area coverage on the heat sink. (See Figure 1)

Regarding claim 4, Glenn discloses the diode projected area coverage on the heat sink is less than the solar cell projected area coverage on the heat sink, and the substrate has a substrate notch, and the by-pass diode is received into the substrate notch. (See Figure 1). It is the position of the examiner to consider the "notch" is a region in the substrate to have the diode. Glenn teaches the substrate having a region for the by-pass diode as shown in Figure 1. Therefore Glenn teaches the limitations of the instant claim, and the reference is deemed to be anticipatory.

Regarding claim 5, Glenn discloses the intermediate-structure projected area coverage on the heat sink is not less than the solar cell projected area coverage on the heat sink. (See Figure 1)

Regarding claim 6, Glenn discloses an intra-unit electrical connection structure (planar tab 14) operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. (See Figures 1).

Regarding claim 7, Glenn teaches the back side of the solar cell is substantially planar. (See Figure 1).

Regarding claim 8, Glenn describes that the solar cell structure includes at least one additional solar cell unit structure as set forth in claim 1, and further including a circuit electrical connection structure (metal trace 19, conducting element 17 and planar

tab 14) operable to electrically interconnect each of the solar cell unit structures in series. (See Figure 1).

Regarding claim 9, Glenn disclose a solar structure as described in claim 1, wherein the solar cell structure includes a joint (metal trace 19 and conducting element 17) between the intermediate structure and the heat sink, and wherein the joint comprises a metallic trace deposited upon a dielectric (bonding 18). (See Figure 1 and col. 5 lines 24-26).

Regarding claim 10, Glenn describes that the solar cell structure includes a joint between the intermediate structure and the heat sink. (See Figure 1). The joint comprises metal trace 19, conducting element 17 and bonding 18. The structure of the joint is indistinguishable to a PC board having a metal trace on a face, therefore the reference is deemed to be anticipatory.

Regarding claim 11, Glenn discloses a solar cell structure 10 having a solar cell unit structure comprising a heat sink (20); a solar cell (11, 12 or 13); an intermediate structure (layers 15-19 between the heat sink 20 and solar cells 11, 12, and 13); an intra-unit electrical connection structure (tab 14). The solar cell has a front side 29, a back side 21, a projected area coverage on the heat sink, and inherently comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated. The intermediate structure is disposed

between and joined to the back side of the solar cell and to the heat sink and having an intermediate-structure projected area coverage on the heat sink. The intermediate structure also comprises a by-pass diode 15 having a diode projected area coverage on the heat sink that is less than the intermediate-structure projected area coverage on the heat sink, and a substrate including layers 16-19 in which layers 16, 17 and 18 are coplanar with the by-pass diode 15. The substrate projected area coverage and the diode projected area coverage on the heat sink taken together are not less than the solar cell projected area coverage on the heat sink. And finally, the intra-unit structure operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. (See Figure 1 and col. 4 lines 24-31)

Regarding claim 12, Glenn describes the back side of the solar cell is substantially planar. (See Figure 1)

Regarding claim 13, Glenn discloses a solar cell structure further including a circuit electrical connection structure (metal trace 19, conducting element 17) operable to electrically interconnect each of the solar cell unit structures in series. (See Figure 1)

Regarding claim 14, Glenn disclose a solar cell structure as described in claim 11, wherein the solar cell structure includes a joint (metal trace 19 and conducting element 17) between the intermediate structure and the heat sink, and wherein the joint

comprises a metallic trace (metal trace 19 or conducting element 17) deposited upon a dielectric layer 18. (See Figure 1 and col. 5 lines 24-26)

Regarding claim 15, Glenn describes that the solar cell structure includes a joint (metal trace 19, conducting element 17 and bonding 18) between the intermediate structure and the heat sink. (See Figure 1). The structure of the joint is not distinguishable to that of a PC board having a metal trace on a face. Therefore, Glenn teaches the limitation of the instant claim and the reference is deemed to be anticipatory.

4. Claims 1, 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Hokuyo et al. (US Patent 4997491).

See Figure 1.

Regarding claim 1, Hokuyo et al. disclose a solar cell structure having a solar cell unit structure comprising a heat sink 403; a solar cell (including layers 201-205) having a front side, a back side, and a solar-cell projected area coverage on the heat sink 403, wherein the solar cell comprises an active semiconductor structure (See col. 4 lines 3-22) that produces a voltage between the front side and the back side when the front side is illuminated; and an intermediate structure (layers 100 and 102) disposed between and joined to the back side of the solar cell and to the heat sink, and having an intermediate-structure projected area coverage on the heat sink, wherein the

intermediate structure comprises a by-pass diode having a diode projected area coverage on the heat sink. (See Figure 1).

Regarding claim 5, Hokuyo et al. disclose the intermediate structure projected area coverage on the heat sink is not less than the solar cell projected area coverage on the heat sink. (See Figure 1).

Regarding claim 6, Hokuyo et al. disclose an intra-unit electrical connection structure (interface between layers 201 and 100) operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. (See Figure 1 and col. 5 lines 24-27).

Regarding claim 7, Hokuyo et al. disclose the back side of the solar cell is substantially planar. (See Figure 1)

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hokuyo et al. (US Patent 4997491).

See Figure 1.

Regarding claim 16, Hokuyo et al. disclose a solar cell structure comprising a heat sink 403; a solar cell (layers 201-205) having a front side, a back side, and a solar-cell projected area coverage on the heat sink, wherein the solar cell comprises an active semiconductor structure that produces a voltage between the front side and the back (See col. 4 lines 22); an intermediate structure (layers 100 and 102) disposed between and joined to the back side of the solar cell and to the heat sink and having an intermediate-structure projected area coverage on the heat sink, wherein the intermediate structure comprises a by-pass diode (including layers 100 and 102) having a diode projected area coverage on the heat sink that is the same as the intermediate-structure projected area coverage on the heat sink, and an intra-unit electrical connection structure (np junction between layers 201 and 100) operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation

(See col. 5 lines 24-27), and a circuit electrical connection structure operable to electrically interconnect each of the solar cell unit structures in series (See col. 5 lines 51-53).

Hokuyo et al. do not explicitly disclose of a solar cell structure having at least two solar cell unit structures in the embodiment.

Hokuyo et al. do teach using a plurality of solar cells, or at least two solar cell unit structures. (See col. 1 lines 17-18)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Hokuyo et al. by using at least two solar unit structure, because using a plurality of solar cells would obtain a voltage which is a sum of voltages of the respective cells. (See col. 1 lines 18-19)

Hokuyo et al. disclose the intermediate structure projected area coverage on the heat sink is not less than the solar cell projected area coverage on the heat sink. (See Figure 1)

Hokuyo et al. describe the back side of the solar cell is substantially planar. (See Figure 1).

8. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hokuyo et al. in view of Glenn (US Patent 6313396).

Regarding claims 19-20, Hokuyo et al. disclose a solar cell structure as described in claim 16.

Hokuyo et al. do not teach that the solar cell structure including a joint between the intermediate structure and the heat sink, wherein the joint comprises a metallic trace deposited upon a dielectric layer, and wherein the circuit electrical connection structure is accomplished in part through the metallic trace, nor do they teach of the joint comprises a PC board having a metal trace on the face.

Glenn teaches the solar cell structure including a joint (metallic trace 19 and conducting element 17) between the intermediate structure and the heat sink, wherein the joint comprise metallic trace deposited upon a dielectric layer 18 and the circuit electrical connection structure is accomplished in part through the metallic trace. (See Figure 1). Further, the structure of the joint taught by Glenn is indistinguishable to that of the PC board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Hokuyo et al. by having a joint between the intermediate structure and the heat sink as taught by Glenn, because it would be inexpensive to manufacture. (See col. 8 line 65 and col. 9 lines 8-13).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh-Truc Trinh whose telephone number is 571-272-6594. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TT
3/21/07

NAM NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700